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NASA TECH BRIEF

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DC-to-AC Inverter Ratio Failure Detector

The problem:

A power system designed to operate in isolated locations contains a triply-redundant central dc-to-ac inverter. An autonomous fault detection-and-correction subsystem is needed to compensate for minimal maintenance. Thus, to maximize power source reliability, a failure detector is needed to switch in the standby inverters. The detector must positively determine true inverter failures and not erroneously switch inverters due to load faults. The inverter is specifically designed to operate with an output overload including a short circuit. The overload, however, pulled down the current-limited input-bus voltage. Thus overloads produced excess input and output currents along with low input and output voltages. In addition, the inverter nominal load changed more than 50 percent, depending on system operating modes. It was therefore apparent that fixed limits, such as excess input currents and low output voltage, could not be directly used.

The solution:

A failure detection technique has been developed based upon input-output ratios, which is independent of inverter loading.

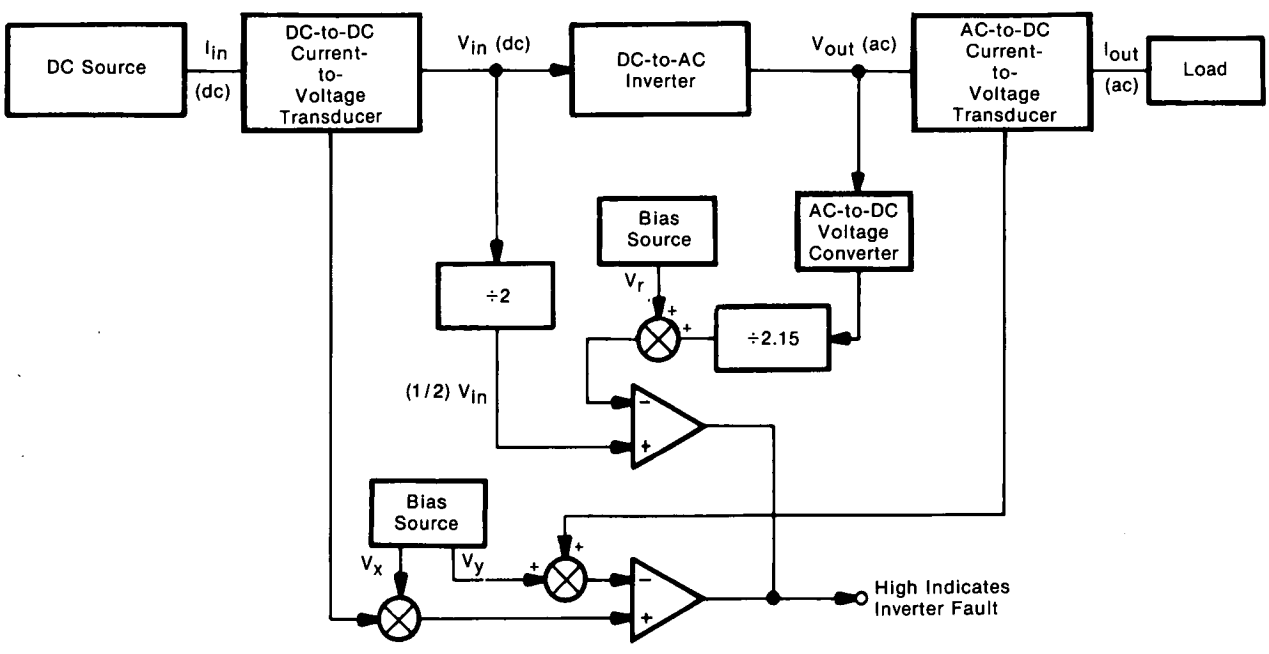

Figure 1. Fault Detector Subsystem

(continued overleaf)

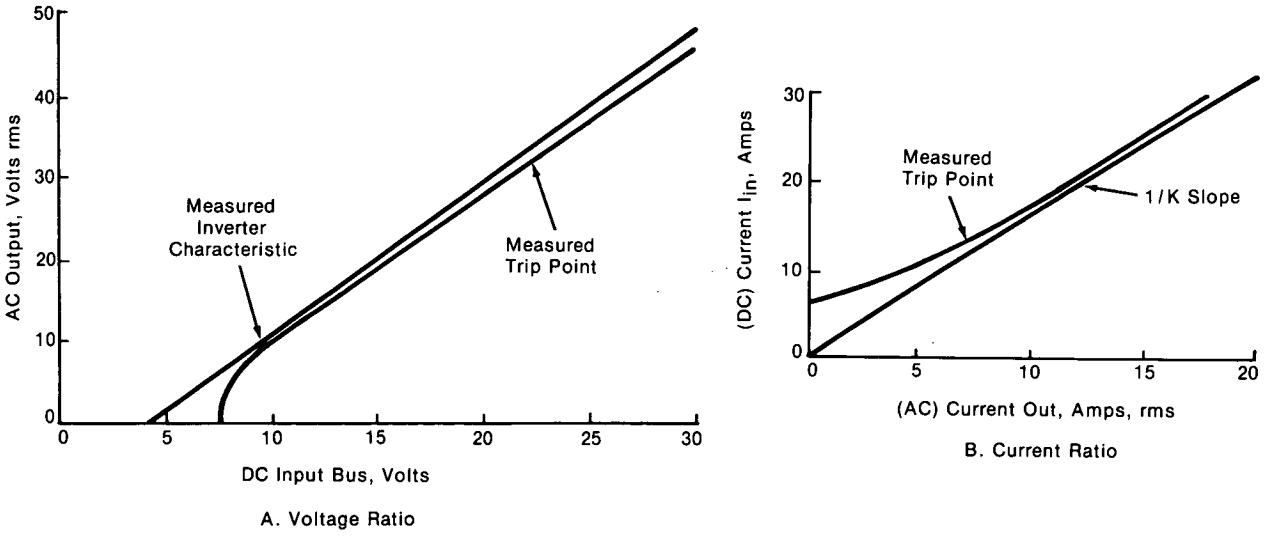

Figure 2. Ratio Fault-Detector, Test Results

How it's done:

Since the inverter has a fixed relationship between V_{in}/V_{out} and I_{in}/I_{out}, the failure detection criteria are based on this ratio, which is simply the inverter transformer turns ratio, K, equal to the primary turns divided by the secondary turns. Inverter failure is defined as

$$V_{out} < (V_{in}/K) - C_1$$

and/or

$$I_{in} > (I_{out}/K) + C_2$$

where C_1 and C_2 are arbitrary constants used to account for sensor offsets and inaccuracies in the hardware implementation. Figure 1 is a block diagram for a particular circuit which satisfies the equations defining inverter failure. A high-gain voltage comparator, such as an operational amplifier, is used to compare the scaled voltages and currents. The constants C_1 and C_2 are approximated by fixed resistors from a constant bias voltage and are represented by the voltages V_r, V_x, and V_y in the diagram.

Figure 2 presents test results of the ratio failure detector. The dropoff of the trip point at low voltage in Figure 2A is required to give an operating margin, due to the variance in inverter characteristics that causes a zero ac output at inputs greater than 4 Vdc. Similarly, the deviation of the trip point at low currents in Figure 2B provides for inverter fixed-losses, such as the oscillator, the drive stages, and the transformer core losses, which require dc input current and yield no ac output current.

Relaxing the trip point settings at low current levels is acceptable, as the limited power source is lightly loaded if the inverter output current is low. The failure detection trip point deviation also allows for inverter efficiency dropoff at low-current levels. Thus, a good lightly loaded inverter is not erroneously tripped off.

Note:

Requests for further information may be directed to:

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Reference: TSP74-10282

Patent status:

This invention has been patented by NASA (U.S. Patent No. 3,795,585). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

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Category: 01 (Electronics - Components and Circuitry)